Title: Formal Verification Engineer (All levels from junior to senior roles)

Description:
In this highly visible role, you will be at the center of a System-on-a-chip (SoC) design verification effort interfacing with design, with a critical impact on getting high quality functional products to millions of customers quickly.

Core Responsibilities:
As a formal verification architect owning the complete formal verification for single or multiple design blocks and IP’s (CPU, Media IP, Security IP, Peripheral IP, Interconnects, Power management subsystems, etc.), you will be responsible for

- Working with SOC and IP design teams to develop a formal micro-architecture specification
- Developing a comprehensive formal verification test plan
- Proving properties of the design, finding design bugs, and working closely with design teams to help improve the micro-architecture
- Architecting novel and innovative solutions for verifying complex design micro-architectures
- Developing and implementing re-usable and optimized formal models and verification code base
- Architecting correct-by-construction design methodologies for improved formal verification efficiency and productivity

Qualifications:
The ideal candidate will have the following experience

- Advanced knowledge of SoC/CPU/GPU designs, VLSI, and digital logic design and verification techniques
- Developed formal property proofs on industrial strength designs and architectures
- Deep understanding of pipeline architectures, memory/DMA controllers, out-of-order and speculative instruction execution hardware, bus interconnects, and cache coherence mechanisms
- Solid understanding of formal verification technologies/abstraction techniques
- Knowledge and experience in interpreting hardware specifications and using temporal logic assertion-based languages such as SVA or PSL
- Experience in using EDA formal tools and tool development experience is a plus
- Proficiency in any scripting language with excellent debugging skills
- Strong team player with excellent communication skills
- Passionate about developing world-class/innovative formal verification solutions

Education: BS / MS / Ph.D in EE or CS or Math or Applied Math is required