

G22.2243-001
High Performance Computer Architecture

Lecture 14
Review

April 26, 2006

Outline

- Announcements
 - Homework assignment 5 and Lab Assignment 5 on the web: **Optional**
 - **Final exam scheduled for next week**
 - Same room (WWH 101)
 - Same time (5pm-7pm)
- Course summary
 - Topics covered
 - Practice questions
 - Exam problems NOT limited to these questions

5/3/2006

2

Grading

- Assignments: 70%
Total points: 520
 - Homeworks
 - Four assignments of equal weight
 - Total points: 120
 - Labs
 - Four assignments of equal weight
 - Total points: 400
- Final Exam: 30%
Total points: 222
 - Two hours
 - 5 or 6 questions
 - Open books, open notes
 - No computers

See me after the class if your grades are not recorded correctly

5/3/2006

3

Course Summary

- | | |
|---|--|
| Preliminaries: | Processor Core |
| • Lecture 1 <ul style="list-style-type: none">– Fundamentals– Technology trends– CPU performance– Amdahl's Law | • Lectures 3-7 <ul style="list-style-type: none">– 5-stage RISC pipeline– Hazards: Structural, Data, Control– Branch prediction<ul style="list-style-type: none">• Static• Dynamic• Hybrid– Dynamic scheduling<ul style="list-style-type: none">• Scoreboarding• Tomasulo's– Speculative execution<ul style="list-style-type: none">• Commit• Reorder buffer– Superscalars: Multiple instruction issue– Limits of ILP– VLIW/EPIC processors<ul style="list-style-type: none">• Software<ul style="list-style-type: none">– Loop unrolling• Hardware<ul style="list-style-type: none">– Conditional/predicated instructions |
| • Lecture 2 <ul style="list-style-type: none">– Instruction set architectures– MIPS | |

5/3/2006

4

Course Summary

- | | |
|---|--|
| Memory Hierarchy | Interconnection Networks (Multiprocessors Cont'd) |
| • Lectures 7-9 <ul style="list-style-type: none">– Caches<ul style="list-style-type: none">• Structure and Performance– Memory<ul style="list-style-type: none">• Organization• Organization-level performance | • Lectures 12 <ul style="list-style-type: none">– Topologies– Routing |
| Multiprocessors | Case studies |
| • Lectures 10-11 <ul style="list-style-type: none">– Current trends– Centralized/decentralized Memory– Communication models for DM<ul style="list-style-type: none">• Shared address space• Private address space (message passing)– Coherence protocol<ul style="list-style-type: none">• Snoopy cache coherence protocols• Directory-based cache coherence– Memory consistency models (briefly) | • Lecture 13 <ul style="list-style-type: none">– IBM and Intel Processors |
| | Review |
| | • Lecture 14 |
| | Plus |
| | • Four lab assignments |
| | • Four homework assignments |

5/3/2006

5

Practice Questions

These questions are meant to provide you with a feeling for the kinds of questions you should expect on the final exam. You can discuss any doubts you may have about your solution on the class mailing list.

- Fundamentals: 1.3, 1.7
- Instruction Set Architectures: 2.1, 2.6, 2.12
- Pipelines: A.5, A.7, A.10
- ILP, Dynamic Scheduling, and Multiple-Issue Processors: A.12, 3.1
- Tomasulo's Algorithm: 3.3, 3.6, 3.10
- Branch Prediction: 3.11
- Hardware-based Speculation: 3.18
- Limitations on ILP: 3.24 (a)
- Loop Unrolling and predication: 4.9, 4.18
- Speculative Memory Access: 4.23 (a, b)
- Memory Hierarchy: 5.4, 5.5
- Multiprocessors: 6.4, 6.10
- Interconnection Networks: 8.18, 8.19

5/3/2006

6