Outline

• Announcements
  – Homework assignment 5 and Lab Assignment 5 on the web: Optional
  – **Final exam scheduled for next week**
    • Same room (WWH 101)
    • Same time (5pm-7pm)

• Course summary
  – Topics covered
  – Practice questions
    • Exam problems NOT limited to these questions
Grading

- Assignments: 70%
  - Total points: 520
    - Homeworks
      - Four assignments of equal weight
      - Total points: 120
    - Labs
      - Four assignments of equal weight
      - Total points: 400
- Final Exam: 30%
  - Total points: 222
    - Two hours
    - 5 or 6 questions
    - Open books, open notes
    - No computers

See me after the class if your grades are not recorded correctly
Course Summary

Preliminaries:

• Lecture 1
  – Fundamentals
  – Technology trends
  – CPU performance
  – Amdahl’s Law

• Lecture 2
  – Instruction set architectures
  – MIPS

Processor Core

• Lectures 3-7
  – 5-stage RISC pipeline
  – Hazards: Structural, Data, Control
  – Branch prediction
    • Static
    • Dynamic
    • Hybrid
  – Dynamic scheduling
    • Scoreboarding
    • Tomasulo’s
  – Speculative execution
    • Commit
    • Reorder buffer
  – Superscalars: Multiple instruction issue
  – Limits of ILP
  – VLIW/EPIC processors
    • Software
      – Loop unrolling
    • Hardware
      – Conditional/predicated instructions
Course Summary

Memory Hierarchy
• Lectures 7-9
  – Caches
    • Structure and Performance
  – Memory
    • Organization
    • Organization-level performance

Multiprocessors
• Lectures 10-11
  – Current trends
  – Centralized/decentralized Memory
  – Communication models for DM
    • Shared address space
    • Private address space (message passing)
  – Coherence protocol
    • Snoopy cache coherence protocols
    • Directory-based cache coherence
  – Memory consistency models (briefly)

Interconnection Networks
(Multiprocessors Cont’d)
• Lectures 12
  – Topologies
  – Routing

Case studies
• Lecture 13
  – IBM and Intel Processors

Review
• Lecture 14

Plus
• Four lab assignments
• Four homework assignments
Practice Questions

These questions are meant to provide you with a feeling for the kinds of questions you should expect on the final exam. You can discuss any doubts you may have about your solution on the class mailing list.

- Fundamentals: 1.3, 1.7
- Instruction Set Architectures: 2.1, 2.6, 2.12
- Pipelines: A.5, A.7, A.10
- ILP, Dynamic Scheduling, and Multiple-Issue Processors: A.12, 3.1
- Tomasulo’s Algorithm: 3.3, 3.6, 3.10
- Branch Prediction: 3.11
- Hardware-based Speculation: 3.18
- Limitations on ILP: 3.24 (a)
- Loop Unrolling and predication: 4.9, 4.18
- Speculative Memory Access: 4.23 (a, b)
- Memory Hierarchy: 5.4, 5.5
- Multiprocessors: 6.4, 6.10
- Interconnection Networks: 8.18, 8.19